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LOCATION: SWANSEA

LLEOLIAD: ABERTAWE

LEVEL 4

LEFEL 4

EXAMINATION PERIOD
MAY 2019

CYFNOD ARHOLIADAU
MAI 2019

HNC / HND IN ELECTRICAL AND ELECTRONIC

MODULE CODE: TBA

Micros Peripherals and Interfaces

TIME: 2 HOURS

ANSWER ALL FIVE QUESTIONS

Equipment or materials required

Instruction set for PIC16f84

Calculators may be used.

Adnoddau neu ddefnyddiau sydd eu hangen -

First Question (10 marks)

1. For the following use the 16F84 instruction set provided.
- a) Determine the status of the Z, C, DC bits in the status register along with the contents of the memory location 0E after the following code segment is run.

```
Post1    equ 0E
;
MOVLW 0x58
MOVWF Post1
MOVLW 0x3A
ADDWF Post1,1
```

(3 marks)

- b) Determine the contents of memory location 14 and the carry bit, after the following code segment is run. (assume that the carry bit is initially = 0)

```
Data1    equ 0x14
;
MOVLW 0x5A
MOVWF Data1
RLF Data1
INCF Data1
RLF Data1
INCF Data1
```

(3 marks)

- c) Change three lines of code in the following code segment so that the subroutine 'Delay1' is called 5 times when the segment is run.

```
Count1    equ 0x12
;
MOVLW 0x06
MOVWF Count1
CALL Delay1
DECF Count1
GOTO Loop
NOP
NOP
```

(4 marks)

Second Question (10 marks)

2.

- a) If a PIC processor has a stack with 8 locations, explain how this would affect the structure of a program written for it.

(3 marks)

- b) Explain the use of subroutines and interrupts in microcontroller programs.

(5 marks)

- c) In order to ensure a program resumes operation in a correct state following an interrupt. What actions would you include within the interrupt routine.

(2 marks)

Third Question (10 marks)

3. a) Explain why it is not possible to connect an a.c. load directly to the output of a 16f84A PIC.

(1 marks)

- b) With the aid of a sketch describe a suitable solution that would allow a PIC to control the ON OFF state of a 230 V a.c. mains operated lamp.

(3 marks)

- c) Explain what precautions need to be taken when reading switched inputs in order to avoid False input.

(3 marks)

- d) How would you connect a switched input to a PIC such that the switch is electrically isolated from the PIC.

(3 marks)

Fourth Question (10 marks)

4. You are provided with a microprocessor with a 10 bit external address bus along with memory devices having only an 8 bit address.

- a) Show how you would connect the memory to the microprocessor such that the entire memory addressing capability of the processor is utilised.

(6 marks)

- b) Show how memory location 875 (decimal) would be accessed.

(4 marks)

Fifth Question (10 marks)

5. Microcontrollers are often required to transfer data between themselves and peripheral devices.

a) Describe 4 key differences between RS232 and SPI interfaces.

(4 marks)

b) A processor is connected to 3 peripheral devices using an I²C interface as shown below in Figure

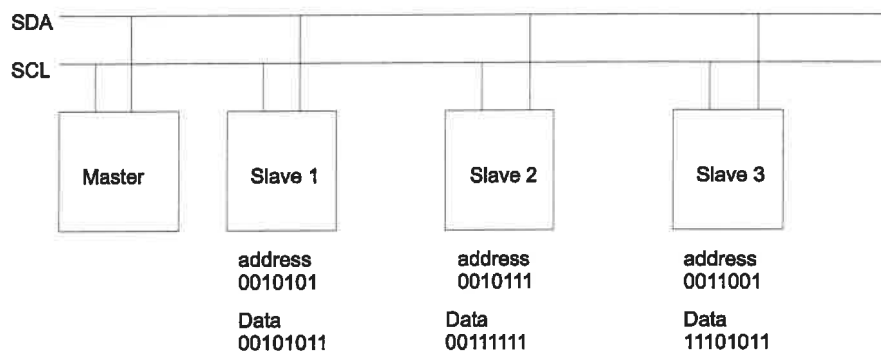


Figure 1

i. How does the Master indicate to the slaves that a message is due to begin

(1 mark)

ii. How does the Master indicate to the slaves that a message is ended

(1 mark)

iii. How does a slave indicate to a master that it is not ready to receive data

(2 marks)

iv. For the network shown in figure 1 above complete the following sequence assuming a successful transfer:

S	0	0	1	1	0	0	1	1											
---	---	---	---	---	---	---	---	---	--	--	--	--	--	--	--	--	--	--	--

(2 marks)

END

Total 50 Marks

PIC16F627A/628A/648A

TABLE 15-2: PIC16F627A/628A/648A INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode				Status Affected	Notes	
			MSb		LSb				
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff ffff	C,DC,Z	1, 2	
ANDWF	f, d	AND W with f	1	00	0101	dfff ffff	Z	1, 2	
CLRF	f	Clear f	1	00	0001	1fff ffff	Z	2	
CLRWF	—	Clear W	1	00	0001	0xxx xxxx	Z		
COMF	f, d	Complement f	1	00	1001	dfff ffff	Z	1, 2	
DECF	f, d	Decrement f	1	00	0011	dfff ffff	Z	1, 2	
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff ffff		1, 2, 3	
INCF	f, d	Increment f	1	00	1010	dfff ffff	Z	1, 2	
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff ffff		1, 2, 3	
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff ffff	Z	1, 2	
MOVF	f, d	Move f	1	00	1000	dfff ffff	Z	1, 2	
MOVWF	f	Move W to f	1	00	0000	1fff ffff			
NOP	—	No Operation	1	00	0000	0xx0 0000			
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff ffff	C	1, 2	
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff ffff	C	1, 2	
SUBWF	f, d	Subtract W from f	1	00	0010	dfff ffff	C,DC,Z	1, 2	
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff ffff		1, 2	
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff ffff	Z	1, 2	
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff ffff		1, 2	
BSF	f, b	Bit Set f	1	01	01bb	bfff ffff		1, 2	
BTFSC	f, b	Bit Test f, Skip if Clear	1(2)	01	10bb	bfff ffff		3	
BTFSS	f, b	Bit Test f, Skip if Set	1(2)	01	11bb	bfff ffff		3	
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk kkkk	C,DC,Z		
ANDLW	k	AND literal with W	1	11	1001	kkkk kkkk	Z		
CALL	k	Call subroutine	2	10	0kkk	kkkk kkkk			
CLRWD ^T	—	Clear Watchdog Timer	1	00	0000	0110 0100	$\overline{TO}, \overline{PD}$		
GOTO	k	Go to address	2	10	1kkk	kkkk kkkk			
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk kkkk	Z		
MOVLW	k	Move literal to W	1	11	00xx	kkkk kkkk			
RETFIE	—	Return from interrupt	2	00	0000	0000 1001			
RETLW	k	Return with literal in W	2	11	01xx	kkkk kkkk			
RETURN	—	Return from Subroutine	2	00	0000	0000 1000			
SLEEP	—	Go into Standby mode	1	00	0000	0110 0011	$\overline{TO}, \overline{PD}$		
SUBLW	k	Subtract W from literal	1	11	110x	kkkk kkkk	C,DC,Z		
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk kkkk	Z		

- Note** 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.
- 3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.